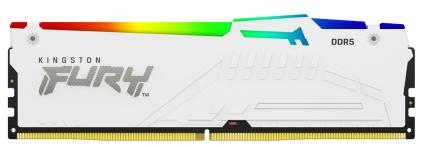
Memory Module Specifications



KF560C36BWE2A-16

16GB 2G x 64-Bit DDR5-6000 CL36 288-Pin DIMM



DEFAULT SPECIFICATIONS

CL(IDD)	40 cycles	
Row Cycle Time (tRCmin)	48ns(min.)	
Refresh to Active/Refresh Command Time (tRFCmin)	295ns(min.)	
Row Active Time (tRASmin)	32ns(min.)	
Row Active Time (tRASmin) UL Rating	32ns(min.) 94 V - 0	
	,	

DESCRIPTION

Kingston FURY KF560C36BWE2A-16 is a 2G x 64-bit (16GB) DDR5-6000 CL36 SDRAM (Synchronous DRAM) 1Rx8, memory module, based on eight 2G x 8-bit FBGA components per module. The module supports AMD® EXPO v1.1 and Intel® Extreme Memory Profiles (Intel® XMP) 3.0. Each module has been tested to run at DDR5-6000 at a low latency timing of 36-44-44 at 1.35V. The SPDs are programmed to JEDEC standard latency DDR5-4800 timing of 40-39-39 at 1.1V. Each 288-pin DIMM uses gold contact fingers. The JEDEC standard electrical and mechanical specifications are as follows:

DEFAULT FEATURES

- Power Supply: VDD = 1.1V Typical
- VDDQ = 1.1V Typical
- VPP = 1.8V Typical
- VDDSPD = 1.8V to 2.0V
- On-Die ECC
- Height 1.66" (42.23mm), w/heatsink

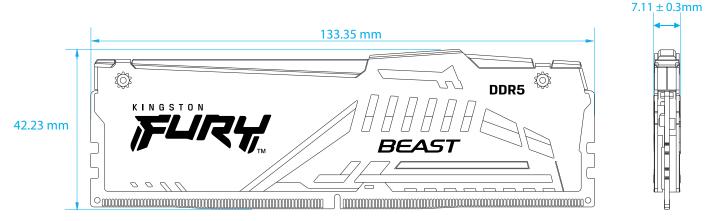
FACTORY TIMING PARAMETERS

Default (JEDEC): DDR5-4800 CL40-39-39 @1.1V
 EXPO Profile #0: DDR5-6000 CL36-44-44 @1.35V
 EXPO Profile #1: DDR5-5600 CL40-40-40 @1.25V
 XMP Profile #1: DDR5-6000 CL36-44-44 @1.35V
 XMP Profile #2: DDR5-5600 CL40-40-40 @1.25V

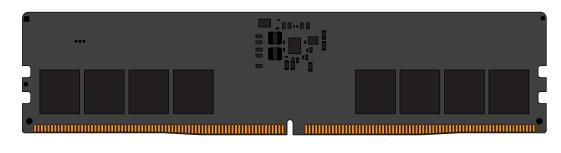
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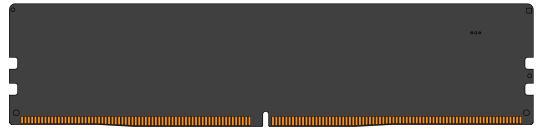


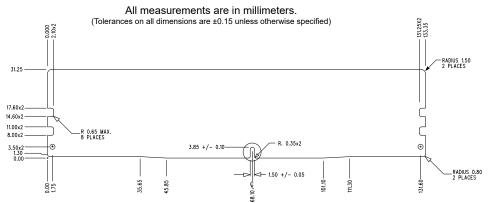
MODULE WITH HEAT SPREADER



MODULE DIMENSIONS







The product images shown are for illustration purposes only and may not be an exact representation of the product. Kingston reserves the right to change any information at anytime without notice.

FOR MORE INFORMATION, GO TO KINGSTON.COM

All Kingston products are tested to meet our published specifications. Some motherboards or system configurations may not operate at the published Kingston FURY memory speeds and timing settings. Kingston does not recommend that any user attempt to run their computers faster than the published speed. Overclocking or modifying your system timing may result in damage to computer components.



Revision No.	History	Release Date	Remark	Editor	Approved
Α	Initial Release	07/12/24		David Y.	Alex S.

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